



Version: 0.6


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# Product Specification

## 2.7" COLOR TFT-LCD MODULE

MODEL NAME: A027CW00\_V0

<  > Preliminary Specification

<            > Final Specification

Note: The content of this specification is subject to change without prior notice.

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### Record of Revision

Version	Revise Date	Page	Content
0.1	MAR/07/2005		First draft
0.2	APR/19/2005	7	Revise VCC & PVDD min voltage to 2.8V
		24	Revise Outline Dimension
0.3	MAY/05/2005	8	Revise V <sub>CDC</sub> , Clock period time, V <sub>sync</sub> to STV input time
		9	Revise Serial clock typical value
		10, 11	Revise The configuration of serial data at SDA
		13, 15,16, 17	Revise Register R2, R4, R5, R6, and Note3
0.4	MAY/23/2005	22	Update Packing form
		23	Revise Outline dimension drawing
0.5	Jun/22/2005	23	Revise Outline dimension drawing – Add FPC thickness
0.6	Jun/30/2005	19	Add 8.Reference Circuit



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**A. Physical specifications**

<b>NO.</b>	<b>Item</b>	<b>Specification</b>	<b>Remark</b>
1	Display resolution (dot)	480(W)×234(H)	
2	Active area (mm)	58.56 (W) × 33.228 (H)	
3	Screen size (inch)	2.65 (Diagonal)	
4	Dot pitch (mm)	0.122 (W) × 0.142 (H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension (mm)	64.60 (W) × 43.50 (H) × 2.01 (D)	Note 1
7	Weight (g)	10.7	
8	Panel surface treatment	Anti-Glare, Hard coating	

Note 1: Refer to Fig. 2

## B. Electrical specifications

### 1.Pin assignment:

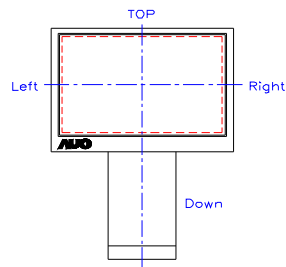
Pin no	Symbol	I/O	Description	Remark
1	DRV	VO	Power transistor gate signal for the boost converter	
2	FB	VI	Main boost regulator feedback input	
3	ADJ0	I	PLL adjustment Pin0	
4	ADJ1	I	PLL adjustment Pin1	
5	PVDD	P	Power supply for PLL circuits (3.3v)	
6	PGND	P	Ground pin for PLL circuits	
7	VA	I	Video R input signal	
8	VB	I	Video G input signal	
9	VC	I	Video B input signal	
10	SCL	I	Serial communication clock input	
11	SDA	I	Serial communication data input	
12	CSB	I	Serial communication chip select	
13	GRB	I	Global reset pin	
14	VSYNC	I	Vertical sync input. Negative polarity	
15	HSYNC	I	Horizontal sync input. Negative polarity	
16	DFRP	O	Digital Frame polarity output signal	
17	AGND	C	Ground pin for source driver	
18	VCI_OUT	C	Power supply for source driver	
19	VCC	P	System power (3.3v)	
20	GND	P	System ground	
21	C1+	C	Power setting capacitor connect pin	
22	C1-	C		
23	C12+	C		
24	C12-	C		
25	C8+	C		
26	C8-	C		
27	V3	C		
28	C31+	C		
29	C31-	C		
30	APOL	O		Frame polarity output signal for panel VCOM
31	VCAC	C	APOL level supply	
32	VGH	C	VGH turn on voltage	
33	VGL	C	Power setting capacitor connect pin	

Pin no	Symbol	I/O	Description	Remark
34	Vgoff_L	C	VGL turn off voltage	
35	Vgoff_H	C	VGL+VCOM	
36	VCOMR	I	Adjust VCOM DC voltage	

### Illustration of I/O symbol

I: Input. O: Output. VI: voltage input. VO: voltage output. P: Power. C: Capacitor pin.

Note 1: Please refer to figure below for the definition of scanning direction.



## 2. Equivalent circuit of I/O

Pin no & Pin name	Schematics
1.DRV	
13.GRB	

## 3. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	$V_{CC}$	GND=0	-0.5	5.	V	
	$AV_{DD}$	$AV_{SS}=0$	-0.5	5.5	V	
Input signal voltage	VCOM		-2.9	5.2	V	
Operating temperature	Topa		0	70	°C	Ambient temperature
Storage temperature	Tstg		-25	80	°C	Ambient temperature

## 4. Electrical characteristics

### a. Typical operating conditions (GND=PGND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply	VCC	2.8	3.3	3.6	V	
	PVDD	2.8	3.3	3.6	V	
	VGH	11.5	14	15	V	Note1.
	VGL	-13.5	-12	-11.5	V	Note1.
	Vgoff_L	-13.5	-12	-11.5	V	Note1.
	Vgoff_H	-9.1	-6.4	-5.7	V	Note1.
	VCI_OUT	4.8	5	5.5	V	Note1.

Video signal Amplitude (VR, VG, VB)		V <sub>iA</sub>	0.2		5.0		
		V <sub>iAC</sub>		3			AC Component
		V <sub>iDC</sub>		2.5			DC Component
		V <sub>I_high</sub>			4.8		Note 2.
Output Signal voltage	H Level	V <sub>OH</sub>	V <sub>CC</sub> -0.4				
	L Level	V <sub>OL</sub>	GND		GND+0.4		
Input Signal voltage	H Level	V <sub>IH</sub>	0.7V <sub>CC</sub>	-	V <sub>CC</sub>	V	
	L Level	V <sub>IL</sub>	GND	-	0.3V <sub>CC</sub>	V	
Output current	H Level	I <sub>OH</sub>		10		uA	
	L Level	I <sub>OL</sub>		-10		uA	
Analog stand by current		I <sub>st</sub>			200	uA	DCLK is stopped
VCOM		V <sub>CAC</sub>	4.4	5.6	5.8	Vp-p	AC component
		V <sub>CDC</sub>		(1.4)			V

Note 1. These voltages (V<sub>GH</sub>, V<sub>GL</sub>, V<sub>goff\_H</sub>, V<sub>goff\_L</sub>, V<sub>CI\_OUT</sub>) are related to input voltage V<sub>CC</sub>.

Note 2. The R,G,B maximum input voltage can not higher than 4.8 volt.

b. Current consumption (GND=AV<sub>SS</sub>=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
	I <sub>CC</sub>	V <sub>CC</sub> =3.3V	-	2	2.5	mA	
	I <sub>DD</sub>	AV <sub>DD</sub> =3.3V	-	1.5	2.0	mA	

## 5. AC Timing

a. NTSC:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Clock period time	t <sub>OSC</sub>	94	104.6	114	ns	
Hsync period time	T <sub>Hs</sub>	61.5	63.5	65.5	us	
Vsync pulse width	T <sub>wvs</sub>	1	-	260	Hs	
Vsync to Hsync timing	T <sub>vshs</sub>	0			ns	Note1
Hsync to Vsync timing	T <sub>hsvs</sub>	0			ns	
Vsync to STV input time	T <sub>vs</sub>	7	19	26	Hs	ref to Fig. 6
Horizontal lines per field		256	262.5	268	line	Note 2

b. PAL:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Clock period time	t <sub>OSC</sub>	94	104.6	114	ns	
Hsync period time	T <sub>Hs</sub>	62	64	66	us	
Vsync pulse width	T <sub>wvs</sub>	1	-	260	Hs	
Vsync to Hsync timing	T <sub>vshs</sub>	0			ns	Note1
Hsync to Vsync timing	T <sub>hsvs</sub>	0			ns	
Vsync to STV input time	T <sub>vs</sub>	12	24	31	Hs	ref to Fig. 6
Horizontal lines per field		306	312.5	318	line	Note 2



Note 1: Vsync and Hsync both support rising edge or falling edge timing

Note 2: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

c. Horizontal Timing:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Hsync frequency	Fhs	-	15.75k	-	Hz	
Hsync pulse width time	Twhs	5	44	600	Tclk	
Hsync to DFRP change time	Thsdfpr	-	40	-	Tclk	
Hsync to APOL change time	Thsapol	-	40	-	Tclk	

Refer to Figure 3.

d. 3-wire serial communication AC timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial clock	Tsck	300	1000		ns
SCL pulse duty	Tscw	40	50	60	%
CSB hold time	Tcst	120			ns
Serial data setup time	Tist	120			ns
Serial data hold time	Tiht	120			ns
Serial clock high/low	Tssw	120			ns
Chip select distinguish	Tcd	1			us
CSB to Vsync Time	Tcv	1			us

Refer to Figure 5.



**6. The configuration of serial data at SDA terminal is at below**

MSB													LSB											
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0																								
Address			X	DATA																				
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default						
R0	0	0	0	X	X	X	X	X	X	X	X	X	X	0	0	0	Select relationship between the inputs VA, VB, VC and outputs R, G, B.	v						
				X	X	X	X	X	X	X	X	X	X	X	0	0			1					
				X	X	X	X	X	X	X	X	X	X	X	X	0			1	0				
				X	X	X	X	X	X	X	X	X	X	X	X	1			0	0				
R1	0	0	1	X	X	X	X	X	X	X	X	X	0	0	0	0	Up to down	v						
				X	X	X	X	X	X	X	X	X	0	0	0	1			Down to up					
				X	X	X	X	X	X	X	X	X	0	0	0	0				Right to left				
				X	X	X	X	X	X	X	X	X	0	0	1	0					Left to right			
				X	X	X	X	X	X	X	X	X	0	0	0	0						In reset state		
				X	X	X	X	X	X	X	X	X	0	1	0	0							Normal	
				X	X	X	X	X	X	X	X	X	0	0	0	0								In standby mode
				X	X	X	X	X	X	X	X	X	1	0	0	0								
R2	0	1	0	X	X	X	X	X	X	X	1	0	0	0	0	Set horizontal position	v							
				X	X	X	X	X	X	X	0	0	0	0	0			1						
				X	X	X	X	X	X	X	0	0	0	0	1			0	0					
				X	X	X	X	X	X	X	0	0	1	0	0			0	0					
				X	X	X	X	X	X	X	0	1	0	0	0			0	0					
				X	X	X	X	X	X	X	X	0	0	0	0			0	0					
R3	0	1	1	X	X	X	X	X	X	X	X	0	0	0	0	0	Set vertical position	v						
				X	X	X	X	X	X	X	X	0	0	0	0	1								
				X	X	X	X	X	X	X	X	0	0	1	0	0								
				X	X	X	X	X	X	X	X	0	1	0	0	0								
				X	X	X	X	X	X	X	X	1	0	0	0	0								
				X	X	X	X	X	X	X	X	X	0	1	0	1								
R4	1	0	0	X	X	X	X	X	X	X	X	0	0	0	1	Adjust the VCOM AC level	v							
				X	X	X	X	X	X	X	X	0	0	1	0									
				X	X	X	X	X	X	X	X	0	1	0	0									
				X	X	X	X	X	X	X	X	0	0	0	0			The APOL polarity, the same as DFRP.						
				X	X	X	X	X	X	X	X	0	0	0	0									
				X	X	X	X	X	X	X	X	1	0	0	0				The APOL polarity will be inverted.					



No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default	
	Address			X	DATA														
R5	1	0	1	X	X	X	X	X	X	X	X	0	0	0	0	0	Data format selected by D1.		
				X	X	X	X	X	X	X	X	0	0	0	0	1	Data format auto selection.	✓	
				X	X	X	X	X	X	X	X	0	0	0	0	0	0	NTSC	✓
				X	X	X	X	X	X	X	X	0	0	0	0	1	0	PAL	
				X	X	X	X	X	X	X	X	0	0	0	0	0	0	Normally display	✓
				X	X	X	X	X	X	X	X	0	0	0	1	0	0	16:9 wide display	
				X	X	X	X	X	X	X	X	0	0	0	0	0	0	Hsync and Vsync input Positive polarity	✓
				X	X	X	X	X	X	X	X	0	1	0	0	0	0	Hsync and Vsync input Negative polarity	
				X	X	X	X	X	X	X	X	0	0	0	0	0	0	Normal display	✓
				X	X	X	X	X	X	X	X	1	0	0	0	0	0	4:3 narrow display	
R6	1	1	0	X	X	X	X	X	X	0	0	0	0	0	0	0	PWM control circuit is shut down.	✓	
				X	X	X	X	X	X	0	0	0	0	0	0	1	PWM circuit is working.		
				X	X	X	X	X	X	0	0	0	0	0	0	0	0	PLL is working.	✓
				X	X	X	X	X	X	0	0	0	0	0	1	0	0	PLL is disabled.	
				X	X	X	X	X	X	1	0	0	0	0	0	0	0	PLL frequency Selection	✓
				X	X	X	X	X	X	0	0	0	0	1	0	0			
				X	X	X	X	X	X	0	0	0	1	0	0	0			
				X	X	X	X	X	X	0	0	1	0	0	0	0			
X	X	X	X	X	X	0	1	0	0	0	0	0	0						

"X" => don't care

## Register detail description

Register **R0**:

Control and switch the relationship between the inputs VA, VB, VC and outputs R, G, B. This function is used to match different types of color filters.

D2	D1	D0	Output (n=1 to 160)			
			R	G	B	
0	0	0	R	G	B	Odd Line
			G	B	R	Even Line
0	0	1	G	B	R	Odd Line
			B	R	G	Even Line
0	1	X	B	R	G	Odd Line
			R	G	B	Even Line
1	0	0	R	G	B	Odd Line
			B	R	G	Even Line
1	0	1	G	B	R	Odd Line
			R	G	B	Even Line
1	1	X	B	R	G	Odd Line
			G	B	R	Even Line

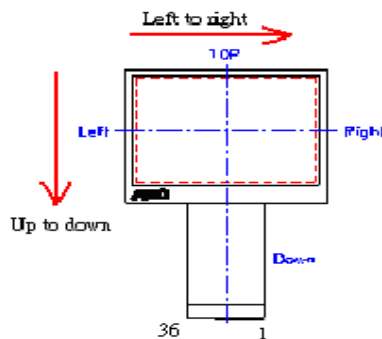
“X” => Regardless

Register **R1**:

Set the scan direction, reset, and standby mode.

Bit	Function
D0	Up/down scan direction. “1”=> Down to up. “0”=> Up to down (Default).
D1	Left/Right scan direction. “1”=> Left to right. (Default) “0”=>Right to left.
D2	Global reset pin, it should be connected to VCC in normal operation. IF connected to GND, the controller is in reset state, normally pulled high.
D3	Standby mode, active low. Normally pulled high.

Default scan direction is below:



Register **R2**:

Set the horizontal position adjustment timing.

D5	D4	D3	D2	D1	D0	NO.	Unit
0	0	0	0	0	0	-32	DCLK
0	0	0	0	0	1	-31	
0	0	0	0	1	0	-30	
0	0	0	0	1	1	-29	
0	0	0	1	0	0	-28	
:	:	:	:	:	:	:	
:	:	:	:	:	:	:	
0	1	1	1	0	1	-3	
0	1	1	1	1	0	-2	
0	1	1	1	1	1	-1	
1	0	0	0	0	0	Default	
1	0	0	0	0	1	+1	
1	0	0	0	1	0	+2	
1	0	0	0	1	1	+3	
:	:	:	:	:	:	:	
:	:	:	:	:	:	:	
1	1	0	1	1	1	+23	
1	1	1	0	0	0	+24	
1	1	1	0	0	1	+25	
1	1	1	0	1	0	+26	
1	1	1	0	1	1	+27	
1	1	1	1	0	0	+28	
1	1	1	1	0	1	+28	
1	1	1	1	1	0	+28	
1	1	1	1	1	1	+28	

Remark: D[5:0]= 111011~111111 will be keep +28 position shift.



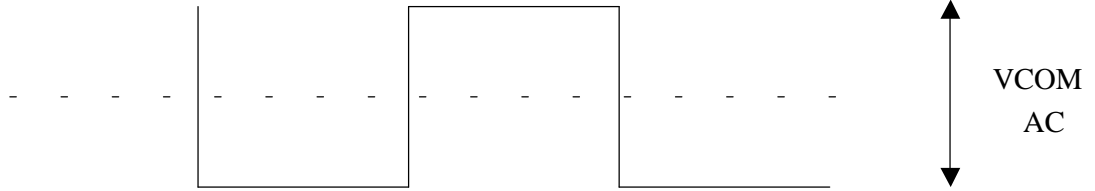
Register **R3**:

Set the vertical position adjustment timing.

D4	D3	D2	D1	D0	NO.	Unit
0	0	0	0	0	Default	H
0	0	0	0	1	+1	
0	0	0	1	0	+2	
0	0	0	1	1	+3	
0	0	1	0	0	+4	
0	0	1	0	1	+5	
0	0	1	1	0	+6	
0	0	1	1	1	+7	
0	1	0	0	0	X	
0	1	0	0	1	X	
0	1	0	1	0	X	
0	1	0	1	1	X	
0	1	1	0	0	X	
0	1	1	0	1	X	
0	1	1	1	0	X	
0	1	1	1	1	X	
1	0	0	0	0	X	
1	0	0	0	1	X	
1	0	0	1	0	X	
1	0	0	1	1	X	
1	0	1	0	0	-12	
1	0	1	0	1	-11	
1	0	1	1	0	-10	
1	0	1	1	1	-9	
1	1	0	0	0	-8	
1	1	0	0	1	-7	
1	1	0	1	0	-6	
1	1	0	1	1	-5	
1	1	1	0	0	-4	
1	1	1	0	1	-3	
1	1	1	1	0	-2	
1	1	1	1	1	-1	

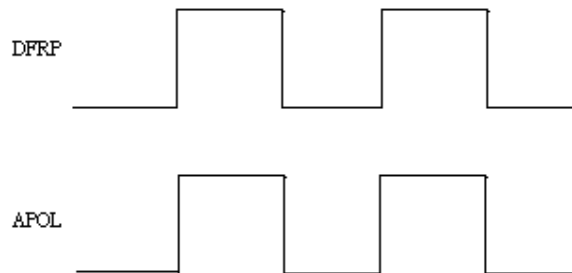
**Register R4:**

D0~D2: Adjust the VCOM AC level.

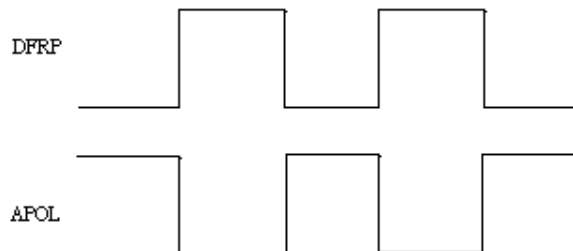


VCAC level setting (Unit: V)			
D2	D1	D0	Level
0	0	0	4.6
0	0	1	4.8
0	1	0	5.0
0	1	1	5.2
1	0	0	5.4
1	0	1	5.6(Default)
1	1	0	5.8
1	1	1	6.0

D3: Set the polarity of APOL. If D3=0, then the polarity of APOL is the same as the polarity of DFRP. As below:



If D3=1, then the polarity of APOL is inverted. As below:



D3	Control APOL are inverted or not, normally pulled low. '0'=>The APOL polarity, the same as DFRP, is negative at the first line. '1'=>The APOL polarity will be inverted.
----	--

**Register R5:**

In this register, the input format of NTSC/PAL is setting here. It would be set by AUTO-selection of external setting. Apart from this 4:3 mode to 16:9 mode is also setting be D2 bit. And the sync polarity could be set by positive and negative.

Bit	Function
D0	Data format auto selection pin, normally pulled high. '1'=>Data format is auto selection. '0'=>Data format is decided by D1.
D1	Data format selection pin, normally pulled low. '1'=>PAL. '0'=>NTSC.
D2	Wide display format selection pin, normally pulled low. '1'=>16:9 wide display. '0'=>Normally display.
D3	Horizontal and vertical sync edge selection, normally pulled low. '0'=>Horizontal and vertical sync input. Positive polarity. '1'=> Horizontal and vertical sync input. Negative polarity.
D4	Narrow display mode selection bit, normally pulled low. '0'=>Normally display. '1'=>4:3 narrow display function enable. S1~S60 and S421~S480 are in black display.

Note: Display mode is normal display when D2='1' and D4='1'.



**Register R6**

In this register, PLL clock is generated by internal synchronize signal. And the PLL frequency can be set to adjust 4:3 circle ratio.

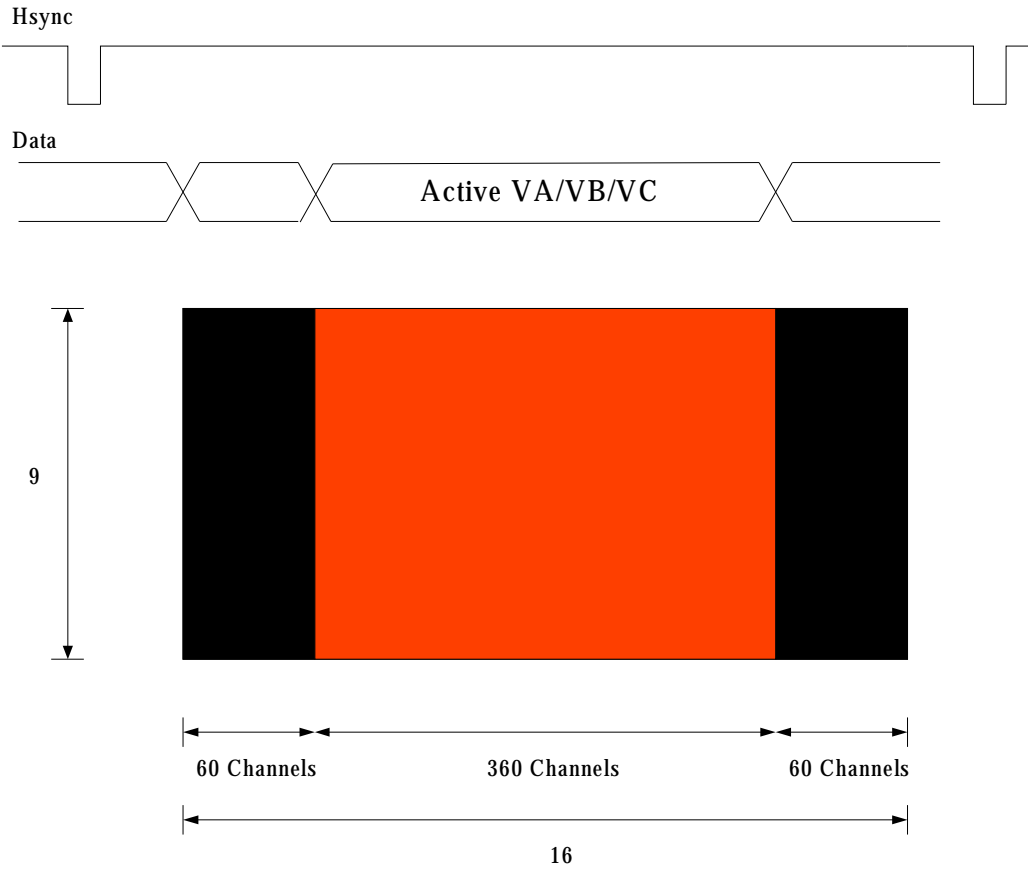
Bit	Function																																																																																																																																																										
D0	Shut down pin for PWM control circuit, normally pulled low. '1'=>PWM control circuit is working normally.. '0'=>PWM control circuit is shut down..																																																																																																																																																										
D1	Disable PLL pin, normally pulled low. '1'=>PLL is disabled and CLK must be input externally. '0'=>CLK is generated by PLL.																																																																																																																																																										
D2~ D6	PLL frequency selection. Note3.																																																																																																																																																										
	<table border="1"> <thead> <tr> <th rowspan="3">D6</th> <th rowspan="3">D5</th> <th rowspan="3">D4</th> <th rowspan="3">D3</th> <th rowspan="3">D2</th> <th colspan="4">Clks no. in Hs</th> <th rowspan="3">Condition</th> </tr> <tr> <th colspan="2">Normally display</th> <th colspan="2">Narrow display</th> </tr> <tr> <th>NTSC</th> <th>PAL</th> <th>NTSC</th> <th>PAL</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>575</td><td>593</td><td>423</td><td>437</td><td rowspan="15">Hsync frequency=15750Hz</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>577</td><td>595</td><td>425</td><td>439</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>579</td><td>597</td><td>427</td><td>441</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>581</td><td>599</td><td>429</td><td>443</td> </tr> <tr> <td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td> </tr> <tr> <td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>605</td><td>623</td><td>453</td><td>467</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>607</td><td>625</td><td>455</td><td>469</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>609</td><td>627</td><td>457</td><td>471</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>611</td><td>629</td><td>459</td><td>473</td> </tr> <tr> <td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td> </tr> <tr> <td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td> </tr> <tr> <td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>633</td><td>651</td><td>481</td><td>495</td> </tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>635</td><td>653</td><td>483</td><td>497</td> </tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>637</td><td>655</td><td>485</td><td>499</td> </tr> </tbody> </table>	D6	D5	D4	D3	D2	Clks no. in Hs				Condition	Normally display		Narrow display		NTSC	PAL	NTSC	PAL	0	0	0	0	0	575	593	423	437	Hsync frequency=15750Hz	0	0	0	0	1	577	595	425	439	0	0	0	1	0	579	597	427	441	0	0	0	1	1	581	599	429	443	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	0	1	1	1	1	605	623	453	467	1	0	0	0	0	607	625	455	469	1	0	0	0	1	609	627	457	471	1	0	0	1	0	611	629	459	473	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	1	1	1	0	1	633	651	481	495	1	1	1	1	0	635	653	483	497	1	1	1	1	1	637	655	485	499
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Note 3. NTSC default setting is 607.

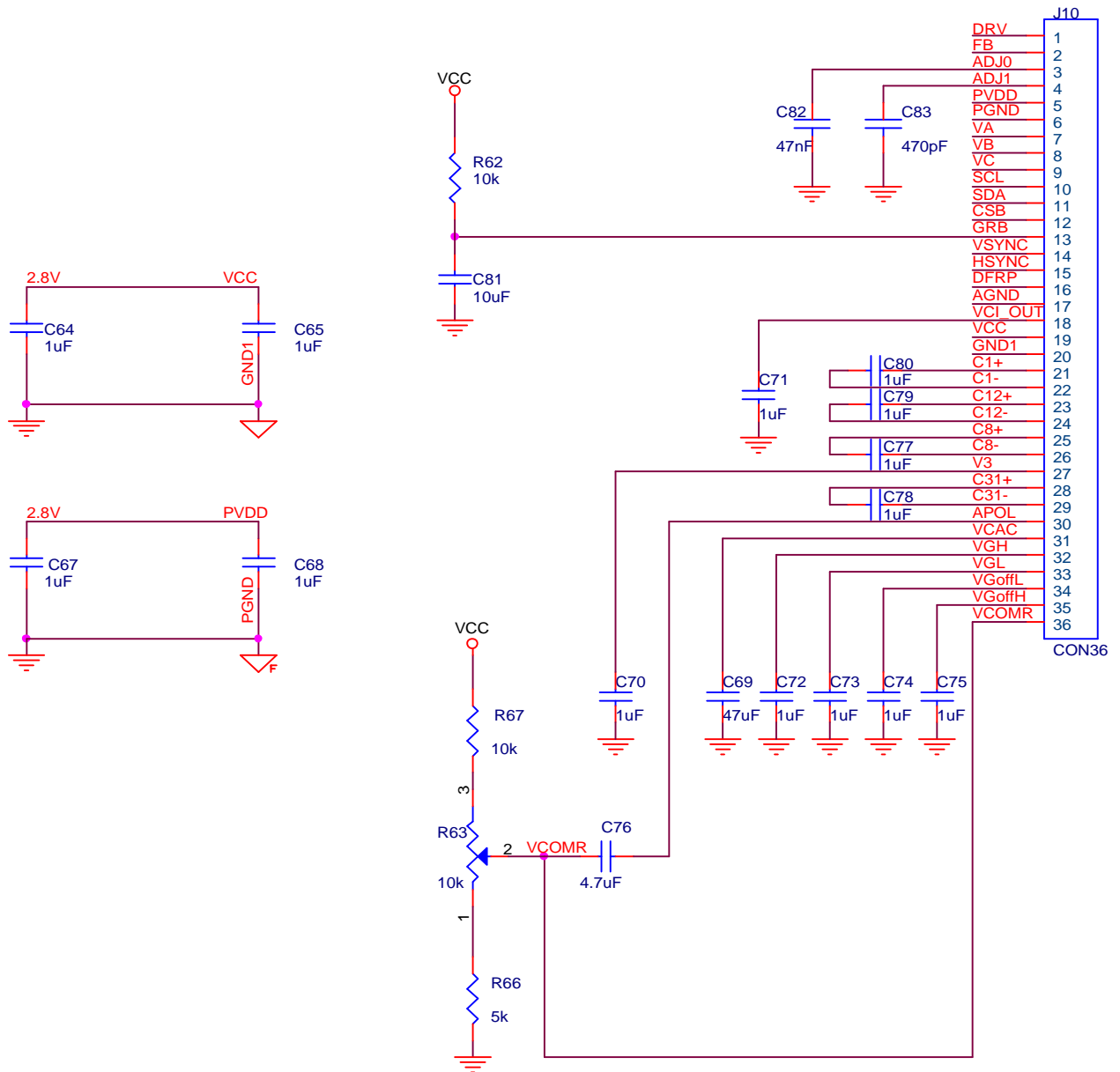
PAL default setting is 625.

### 7. 4:3 Narrow display

In order to display the 4:3 format in 16:9 panel, front 60 channels and last 60 channels must be in black display. Active region will display in center 360 channels.



### 8. Reference Citcuit



**C. Optical specification (Note 1, Note 2, Note 3)**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	$\theta = 0^\circ$	-	20	30	ms	Note 4, 6
	Fall		-	30	40	ms	
Contrast ratio	CR	At optimized viewing angle	100	150	-		Note 5, 6
Viewing angle	Top	$CR \geq 10$	10	-	-	deg.	Note 6, 7
	Bottom		30	-	-		
	Left		40	-	-		
	Right		40	-	-		
Transmittance	$Y_L$	$\theta = 0^\circ$	-	9.5	-	%	Note 8
Color chromaticity	Rx	$\theta = 0^\circ$	--	TBD	--		Note 9
	Ry		--	TBD	--		
	Gx		--	TBD	--		
	Gy		--	TBD	--		
	Bx		--	TBD	--		
	By		--	TBD	--		

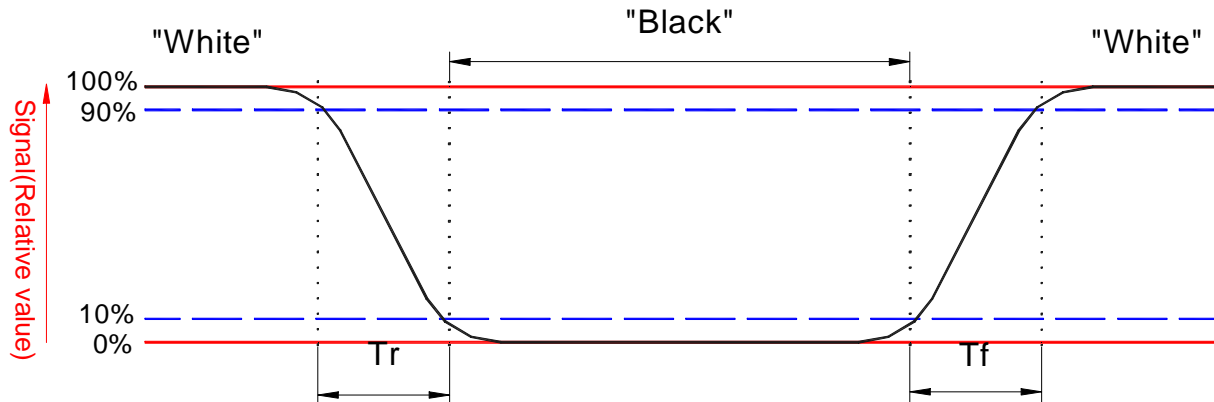
Note 1. Ambient temperature =25°C.

Note 2. To be measured in the dark room.

Note 3. To be measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White  $V_i = V_{i50} \mp 1.5V$

Black  $V_i = V_{i50} \pm 2.0V$

“±” Means that the analog input signal swings in phase with COM signal.

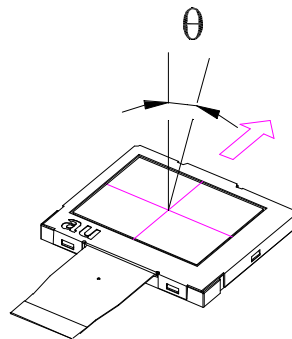
“∓” Means that the analog input signal swings out of phase with COM signal.

$V_{i50}$ : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:

Refer to figure as below.



Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

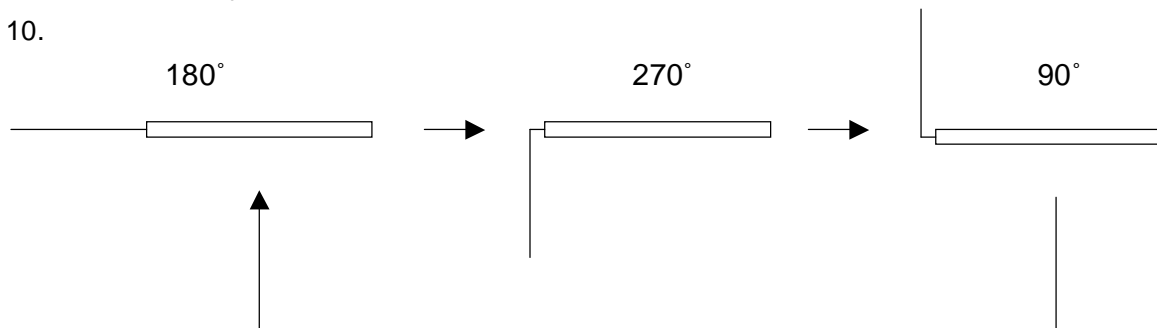
Note 9. To be measured under Backlight chromaticity of (x,y)

**D. Reliability test items:**

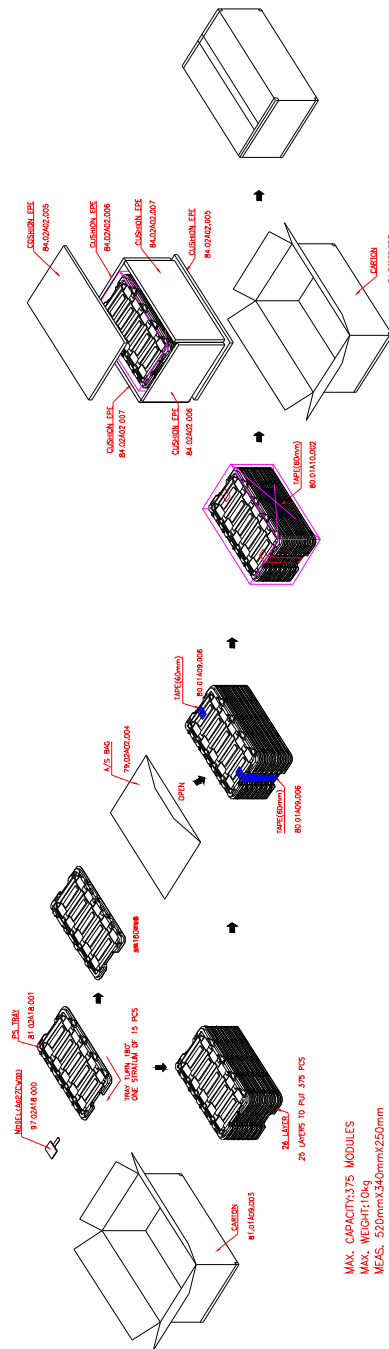
No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80°C 240Hrs	
2	Low temperature storage	Ta= -25°C 240Hrs	
3	High temperature operation	Ta= 60°C 240Hrs	
4	Low temperature operation	Ta= 0°C 240Hrs	
5	High temperature and high humidity	Ta= 60°C . 90% RH 240Hrs	Operation
6	Heat shock	-25°C~80°C/50 cycle @ 2hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz	JIS C7021, A-10 condition A
		Stoke : 1.5mm	
		Sweep : 10~55Hz~10Hz	
		2 hours for each direction of X, Y, Z (6 hours for total)	
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: 0.015G <sup>2</sup> /Hz from 5~200Hz -6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 80cm 1 corner, 3 edges, 6 surfaces	
12	The copper's strength for FPC	The strength is larger 0.7 kg/cm	IPC TM650
13	The film's strength for FPC	The strength is larger 0.35 kg/cm	IPC TM650
14	Flexibility for FPC	1. curved radius: 2mm 2. banding angle: 180° à 270° à 90° à 180° for 50 cycles (Note 10.) 3. Pulling force: 250g	MIT folm: Diagram of test set up for folding endurance

Note: Ta: Ambient temperature.

Note 10.



## E. Packing form



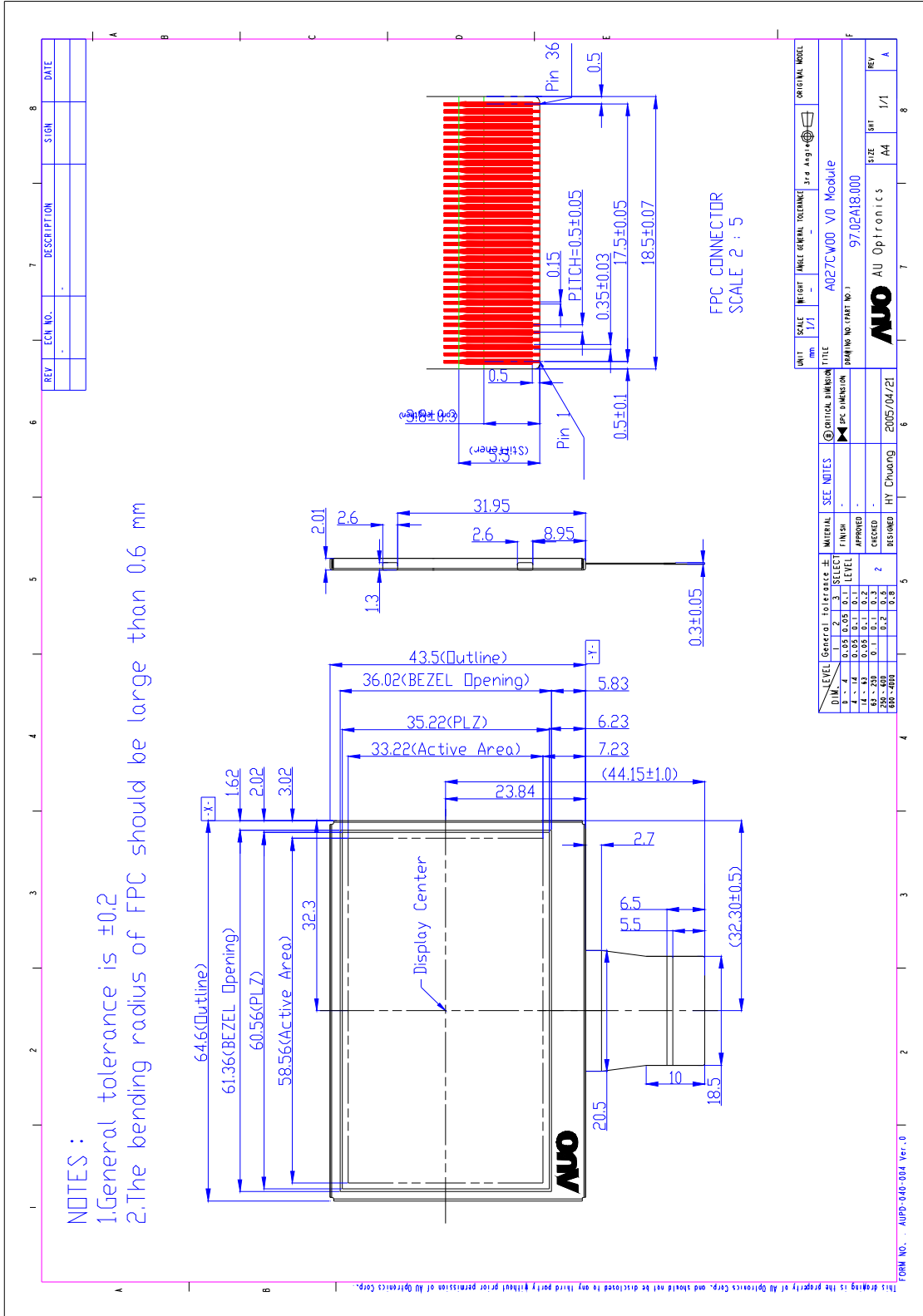


Fig.2 Outline dimension of TFT-LCD module



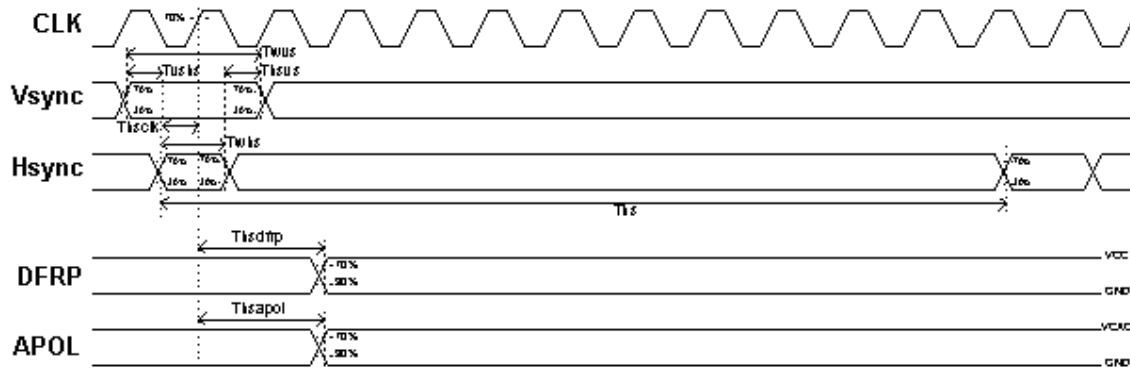


Fig .3 Horizontal Timing Diagram

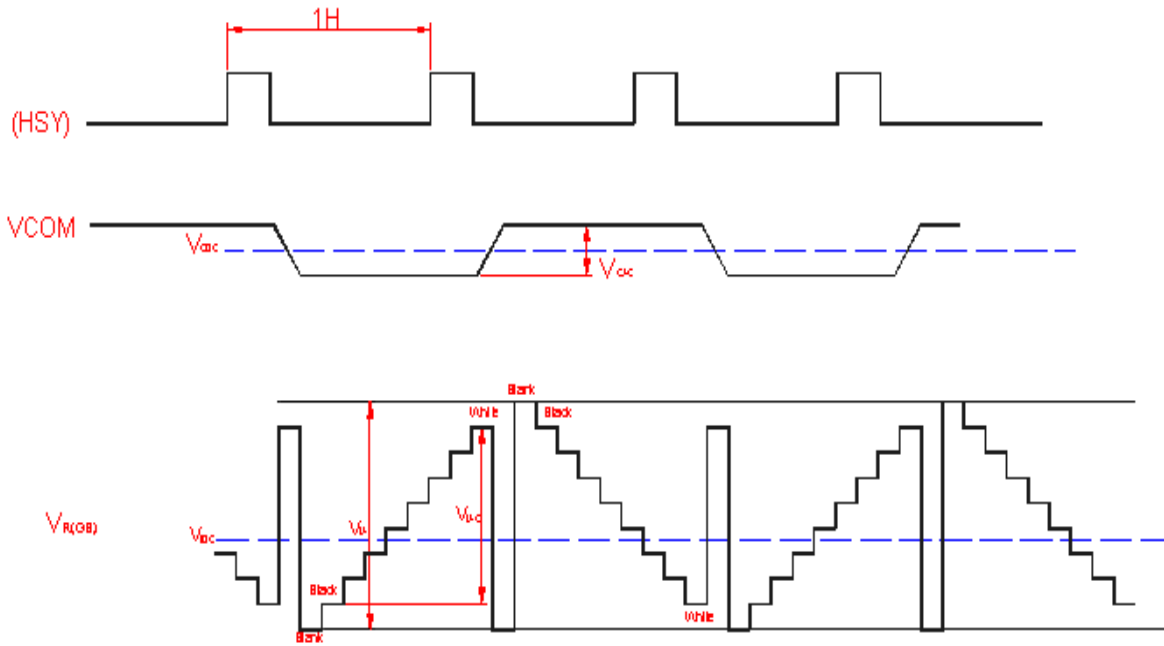
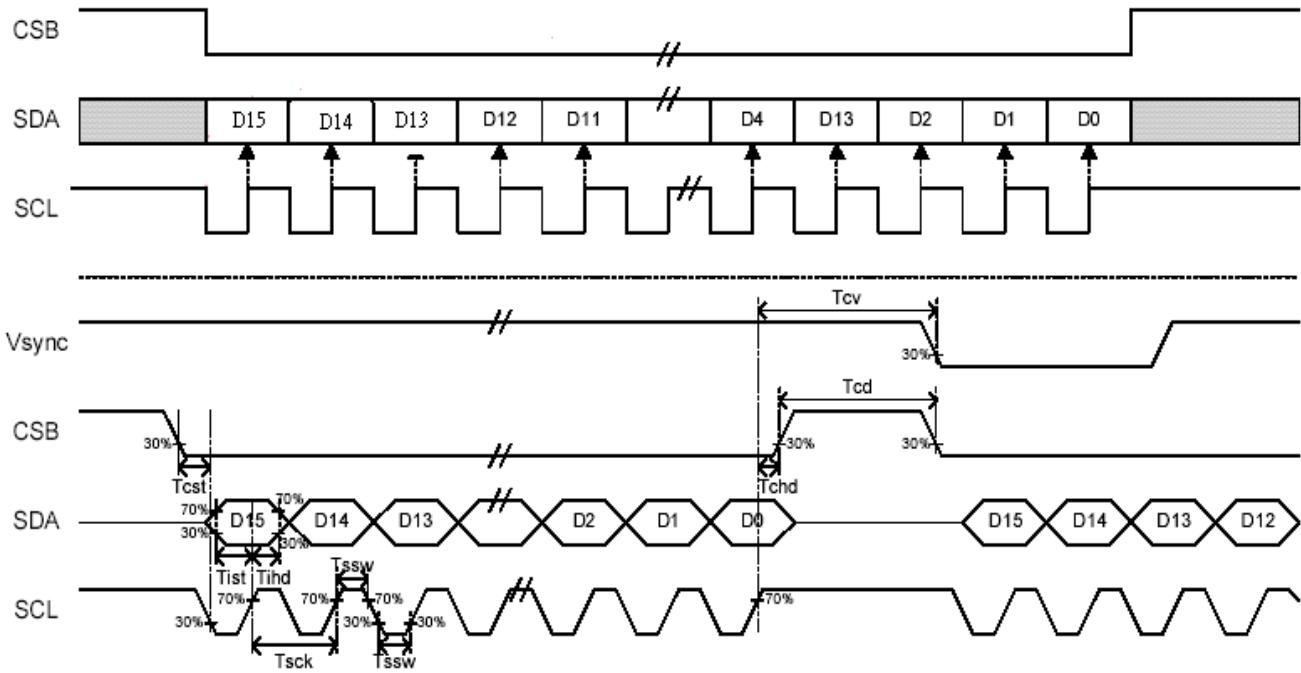
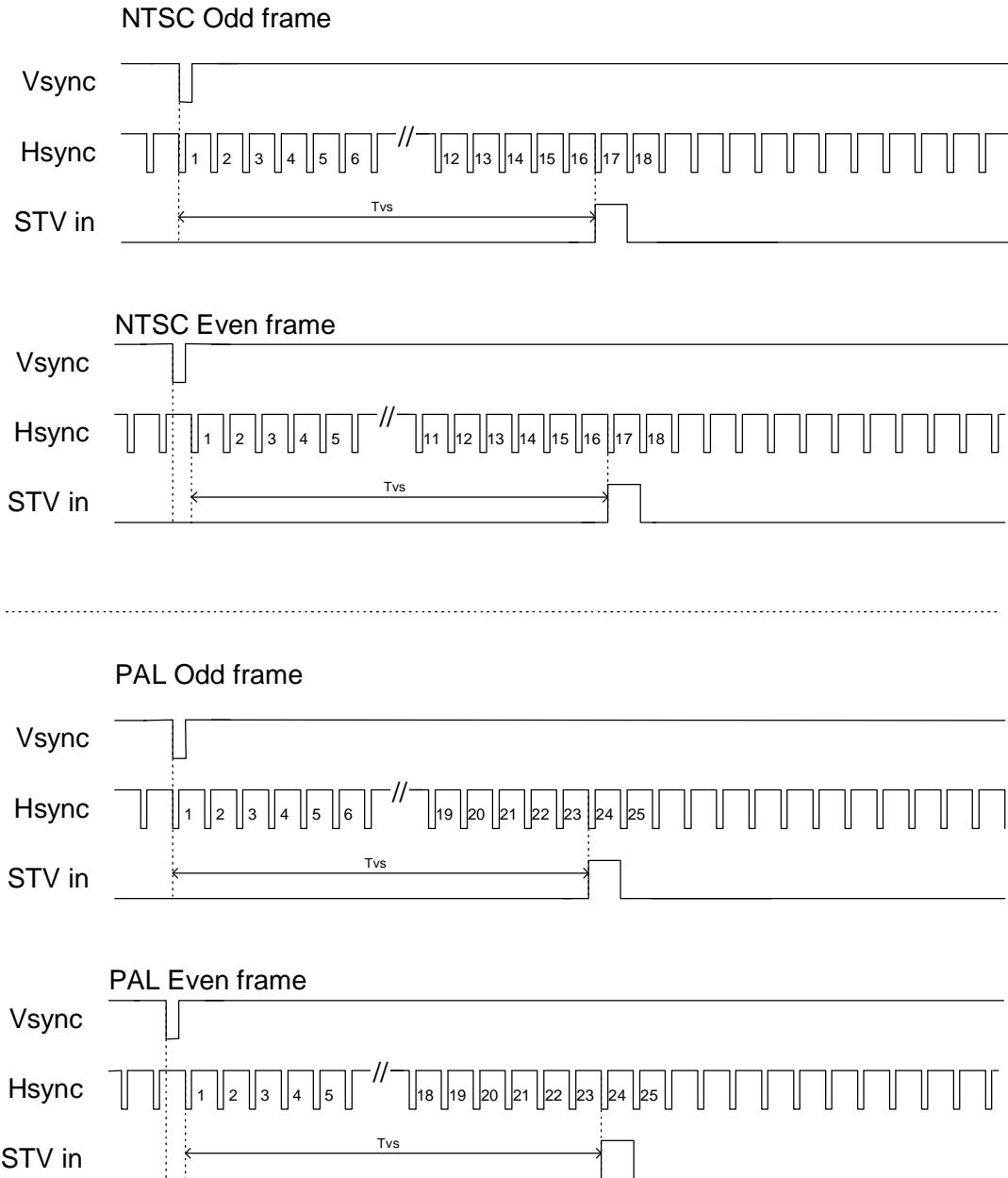


Fig. 4 Input Video signal



**Fig. 5 3-wire programming function Timing**



**Fig. 6 Vertical Timing Diagram**